REMARKS

Summary of the Office Action

In the Non-Final Office Action dated August 2, 2002, claims 15-18 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 15-18 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Japanese Patent No. 10-233397 to Sudipto (hereinafter Sudipto).

Summary of the Response to the Office Action

Claims 15-18 have been amended. Claims 15-18 are currently pending and under consideration.

The Rejection under 35 U.S.C. §112

Claims 15-18 stand rejected under 35 U.S.C. §112, second paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. This rejection is respectfully traversed.

Claims 15-18 have been amended in accordance with the Examiner's comments and to correct any minor informalities indicated by the Examiner. Applicant respectfully submits that claims 15-18 fully comply with the requirements of 35 U.S.C. §112, second paragraph. Accordingly, Applicant respectfully request that the rejection of claims 15-18 under 35 U.S.C. §112, second paragraph be withdrawn.

The Rejection under 35 U.S.C. §102

Claims 15-18 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Sudipto.

To the extent that the Examiner may consider this rejection to apply to the newly amended claims, the rejection is traversed as being based upon a reference that neither teaches nor suggests the novel combination of features recited in the claims.

Independent claims 15-18 recite a semiconductor device, including amongst other novel features, a nonconductive layer contacting and covering the first insulating layer.

The Office Action relies upon Fig. 1a of Sudipto for an alleged teaching of a first wiring layer (28) composed of a plurality of wiring patterns separated from each other embedded in a first insulating layer (22), a nonconductive layer (30) contacting the first wiring layer (28) and covering the first insulating layer (22). Although it is alleged that Sudipto discloses an nonconductive layer (30) covering an alleged first insulating layer (22), the alleged nonconductive layer (30) does not contact the alleged first insulating layer (22). Therefore, Sudipto fails to disclose or teach at least the feature of a nonconductive layer contacting the first wiring layer, and contacting and covering the first insulating layer, as recited in newly amended claims 15-18. Furthermore, Sudipto teaches removing an oxidized copper area or overfilling area 30 by using etching or chemical mechanical polishing (CMP). Contrary to Sudipto the present invention skips this step, and rather than removing the overfill area, the present invention changes the property of the area.

Accordingly, Applicant respectfully asserts that the rejection under 35 U.S.C. §102(e) should be withdrawn because Sudipto does not teach or suggest each feature of independent

claims 15-18. As pointed out in MPEP §2131, "[t]o anticipate a claim, the reference must teach every element of the claim." Thus, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987)." Therefore, Applicant respectfully requests that the rejection of claims 15-18 be withdrawn and the allowance of claims 15-18 is respectfully requested.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully requests reconsideration of this application, withdrawal of all rejections, and the timely allowance of all pending claims 15-18.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite the prosecution.

EXCEPT for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 50-0310. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 15-18 have been amended as follows:

15. (Three Times Amended) A semiconductor device comprising:

a first wiring layer composed of a plurality of wiring patterns separate from each other embedded ~~[and wired on an upper surface of]~~ **on** a first insulating layer which covers a surface of a semiconductor substrate;

a nonconductive layer ~~[formed by oxidation of material composing]~~ **contacting and covering the first insulating layer and contacting** the first wiring layer, ~~[wherein the nonconductive layer comes into contact with the first wiring layer and covers the first insulating layer, and]~~ a top of the first wiring layer ~~[is]~~ not higher than a top of the first insulating layer, further wherein thickness of said nonconductive layer being arranged above the wiring layer is thicker than that of being arranged above the insulating layer.

16. (Twice Amended) A semiconductor device, comprising:

a substrate;

a first insulating layer covering a surface of the substrate;

a first wiring layer including a plurality of wiring patterns separate from each other embedded ~~[and wired]~~ on an upper surface of the first insulating layer, the first wiring layer including a first material; and

a ~~[nonconductive layer formed by oxidation of the first material, the]~~ nonconductive layer contacting the first wiring layer**, and contacting** and covering the first insulating layer,

wherein a top of the first wiring layer is not higher than a top of the first insulating layer, and a thickness of said nonconductive layer being arranged above the wiring layer is thicker than that of being arranged above the insulating layer.

17. (Twice Amended) A semiconductor device, comprising:

a substrate;

a first insulating layer covering a surface of the substrate;

a first wiring layer including a plurality of wiring patterns separate from each other embedded ~~[and wired]~~ on an upper surface of the first insulating layer; and

a nonconductive layer contacting the first wiring layer**, and contacting** and covering the first insulating layer, the nonconductive layer includes oxygen ions,

wherein a top of the first wiring layer is not higher than a top of the first insulating layer, and a thickness of said nonconductive layer being arranged above the wiring layer is thicker than that of being arranged above the insulating layer.

18. (Twice Amended) A semiconductor device, comprising:

a substrate,

a first insulating layer covering a surface of the substrate;

a first wiring layer including a plurality of wiring patterns separate from each other and embedded on an upper surface of the first insulating layer; and

a nonconductive layer that includes oxygen ions contacting the first wiring layer**, and contacting** and covering the first insulating layer,

wherein ~~[a top of the first wiring layer is not higher than a top of the first insulating layer, and a thickness of said nonconductive layer being arranged above the wiring layer is thicker than that of being arranged above the insulating layer]~~ **at least one of the wiring patterns includes at least one capacitor formed therein**.